FIG. 1

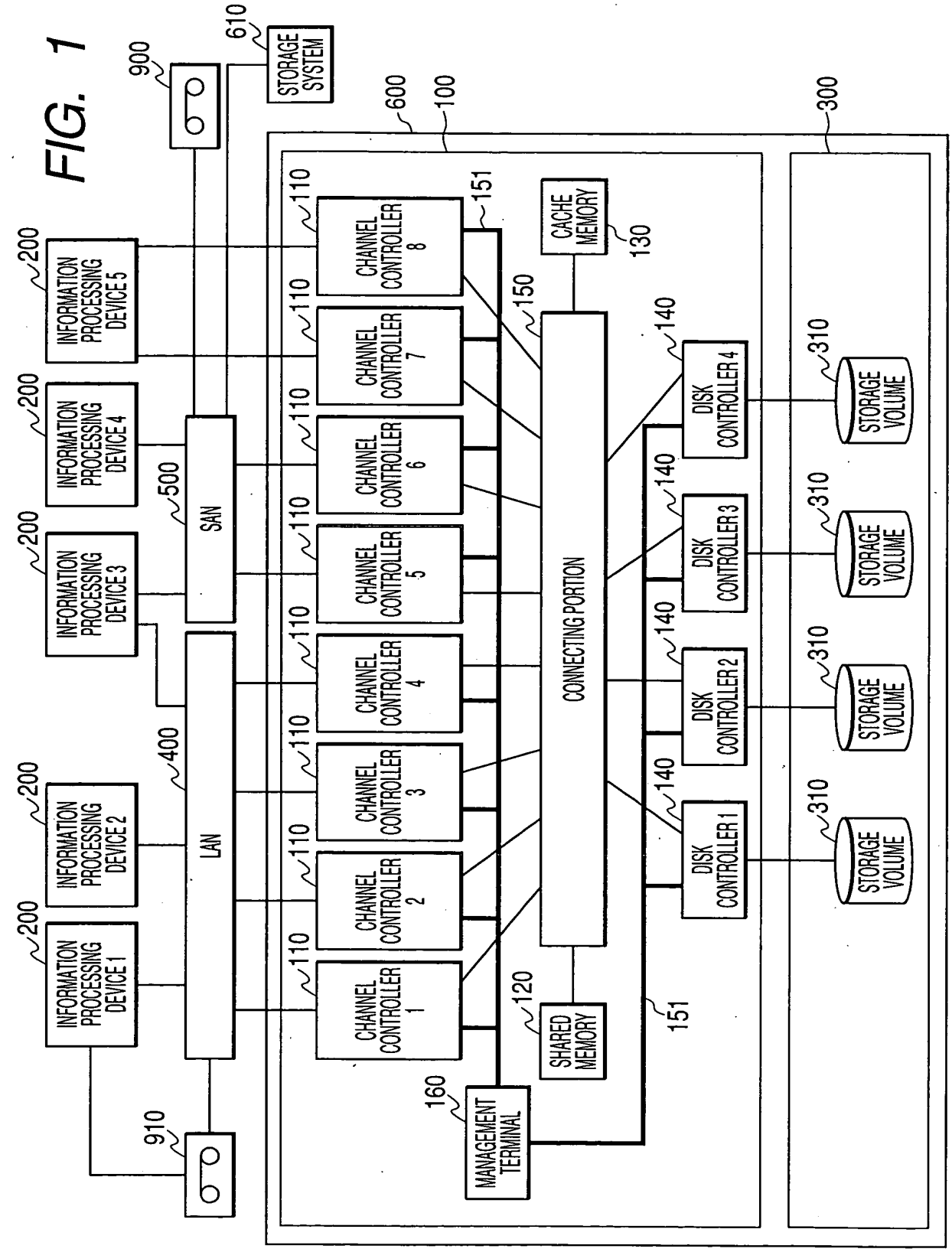

INFORMATION PROCESSING DEVICE 1
INFORMATION PROCESSING DEVICE 2
INFORMATION PROCESSING DEVICE 3
INFORMATION PROCESSING DEVICE 4
INFORMATION PROCESSING DEVICE 5
200
LAN
400
SAN
500
910
900
STORAGE SYSTEM
610
600
100
300
CHANNEL CONTROLLER 1
CHANNEL CONTROLLER 2
CHANNEL CONTROLLER 3
CHANNEL CONTROLLER 4
CHANNEL CONTROLLER 5
CHANNEL CONTROLLER 6
CHANNEL CONTROLLER 7
CHANNEL CONTROLLER 8
110
CONNECTING PORTION
150
CACHE MEMORY
130
SHARED MEMORY
120
MANAGEMENT TERMINAL
160
151
DISK CONTROLLER 1
DISK CONTROLLER 2
DISK CONTROLLER 3
DISK CONTROLLER 4
140
STORAGE VOLUME
310

FIG. 2

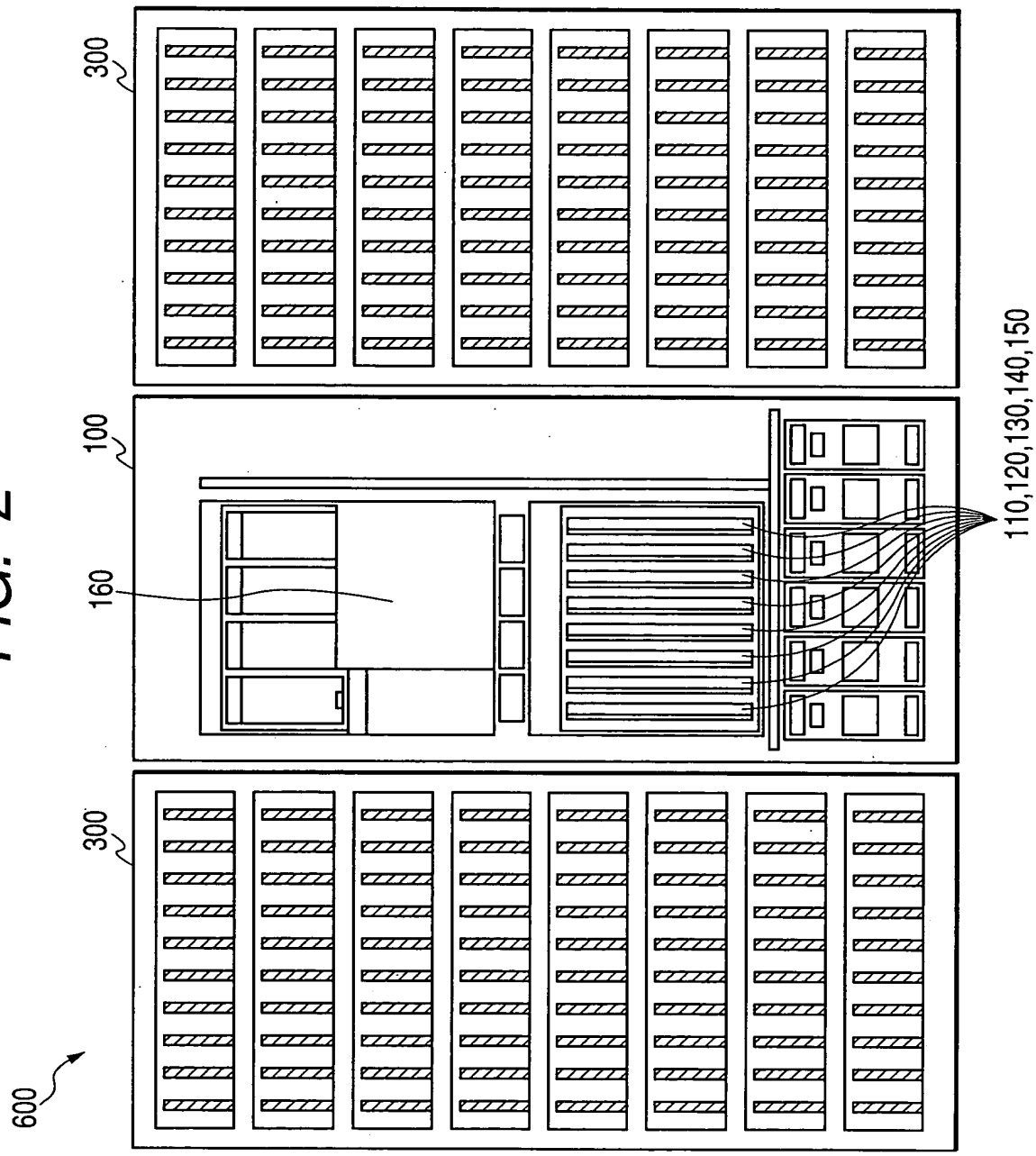


FIG. 3

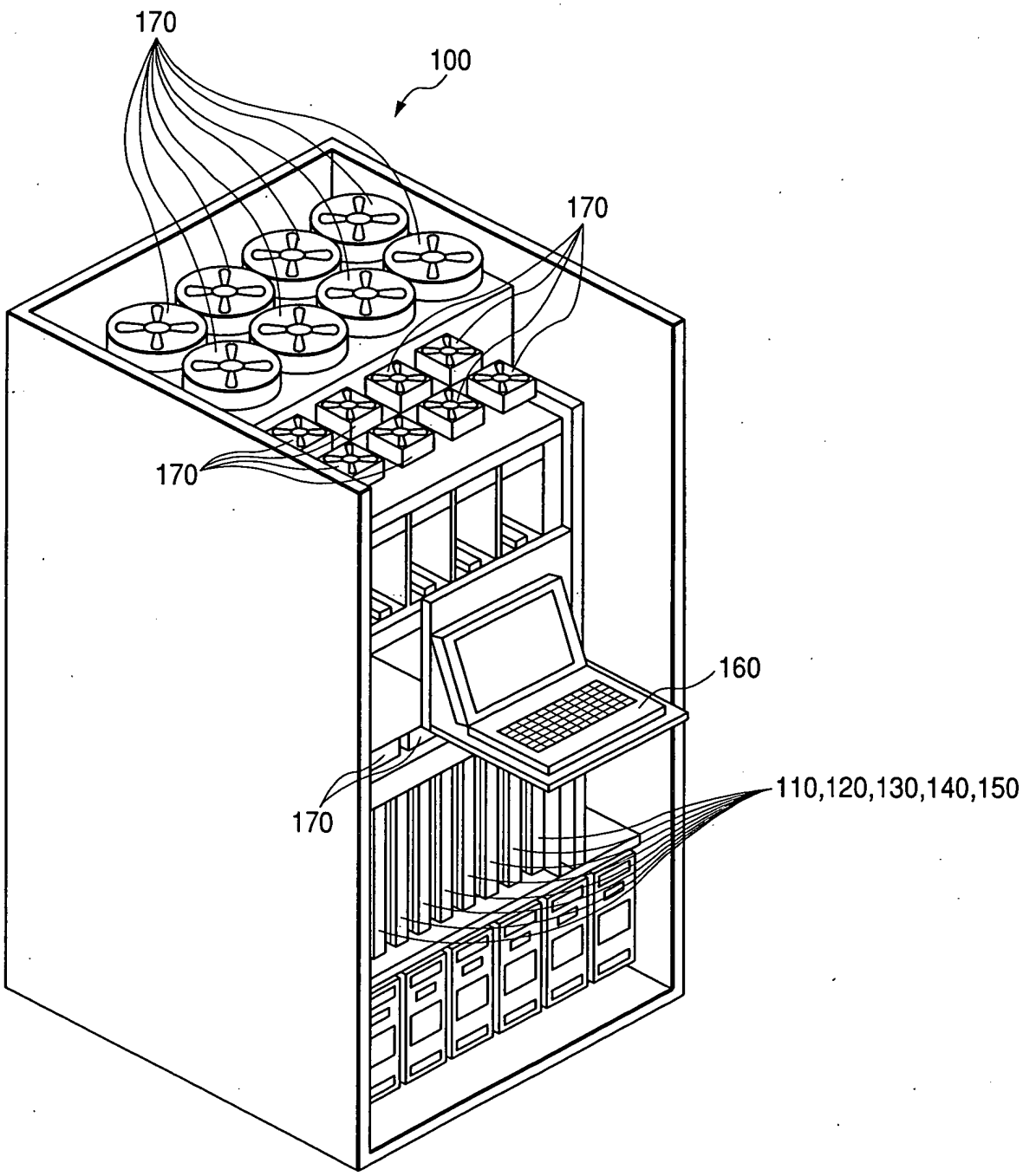


FIG. 4

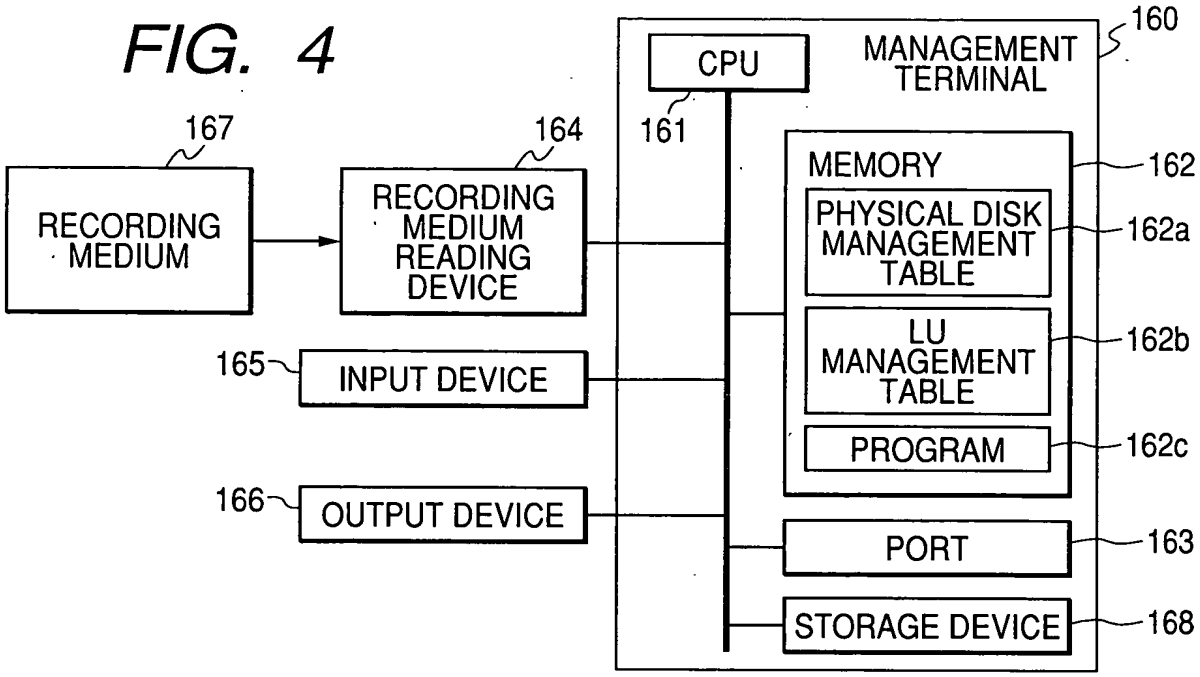


FIG. 5

162a PHYSICAL DISK MANAGEMENT TABLE

DISK NUMBER	CAPACITY	RAID	USE CONDITION
#001	100GB	5	OCCUPIED
#002	100GB	5	OCCUPIED
#003	100GB	5	OCCUPIED
#004	100GB	5	OCCUPIED
#005	100GB	5	OCCUPIED
#006	50GB	—	UNOCCUPIED
⋮	⋮	⋮	⋮

FIG. 6

162b LU MANAGEMENT TABLE

LU NUMBER	PHYSICAL DISK	CAPACITY	RAID
#1	#001,#002,#003,#004,#005	100GB	5
#2	#001,#002,#003,#004,#005	300GB	5
#3	#006,#007,	200GB	1
⋮	⋮	⋮	⋮

FIG. 7

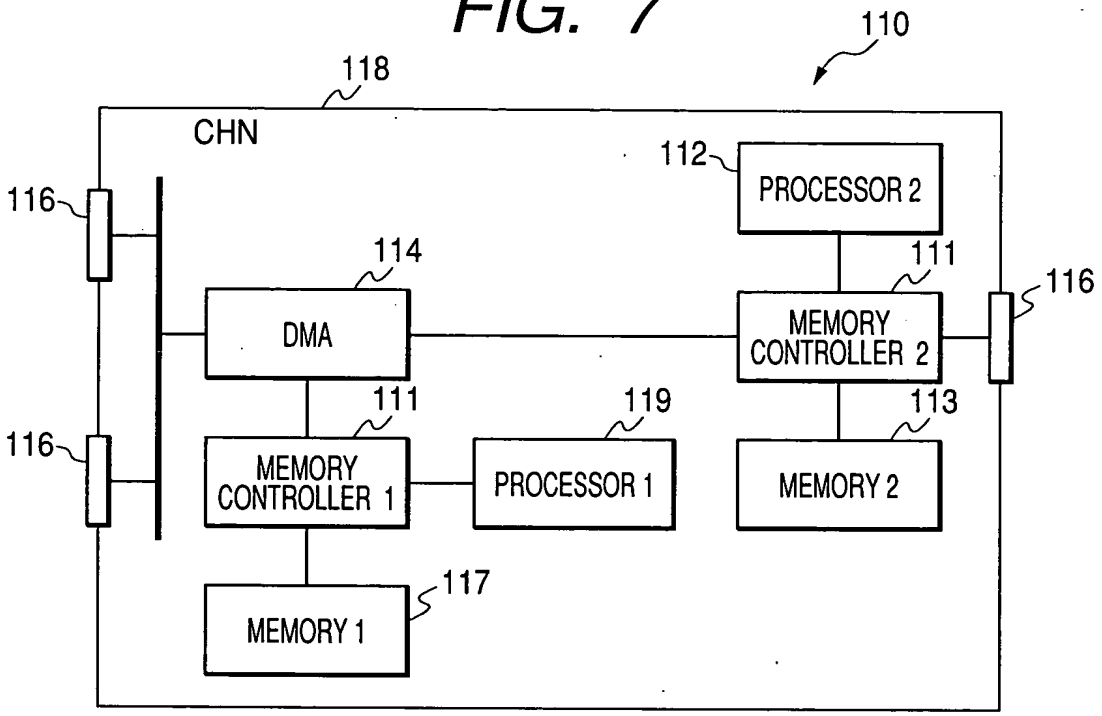

110
118
CHN
112
PROCESSOR 2
116
114
111
116
DMA
MEMORY CONTROLLER 2
111
119
113
116
MEMORY CONTROLLER 1
PROCESSOR 1
MEMORY 2
117
MEMORY 1

FIG. 8

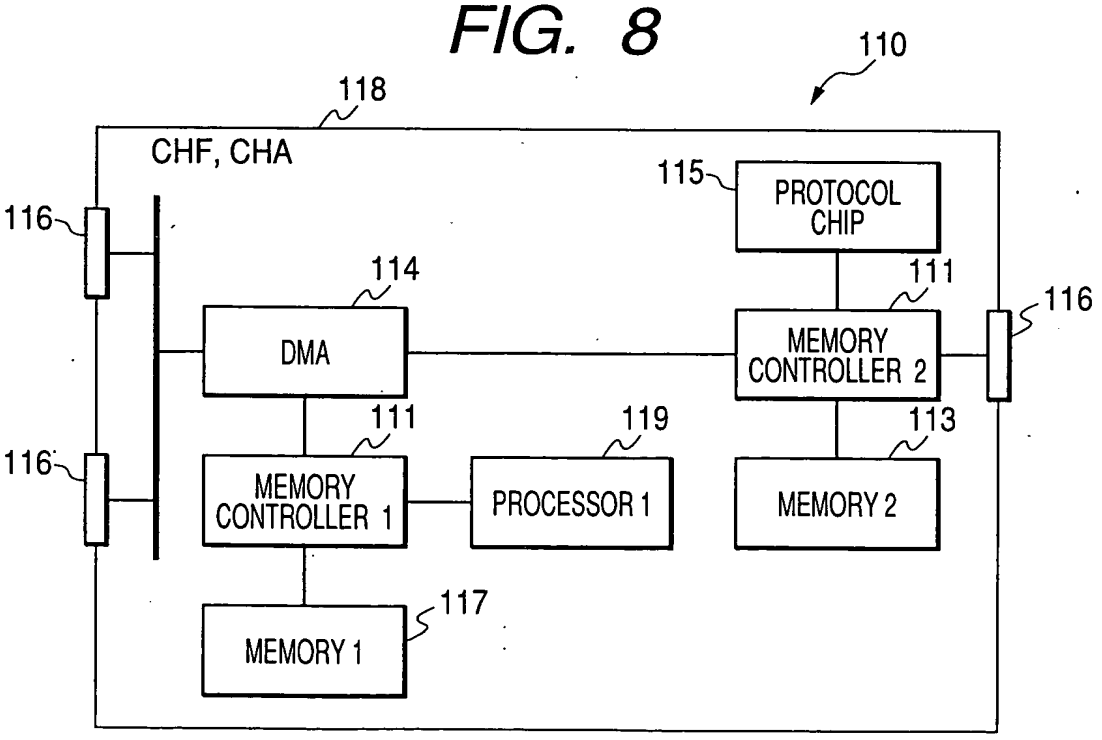

110
118
CHF, CHA
115
PROTOCOL CHIP
116
114
111
116
DMA
MEMORY CONTROLLER 2
111
119
113
116
MEMORY CONTROLLER 1
PROCESSOR 1
MEMORY 2
117
MEMORY 1

FIG. 9

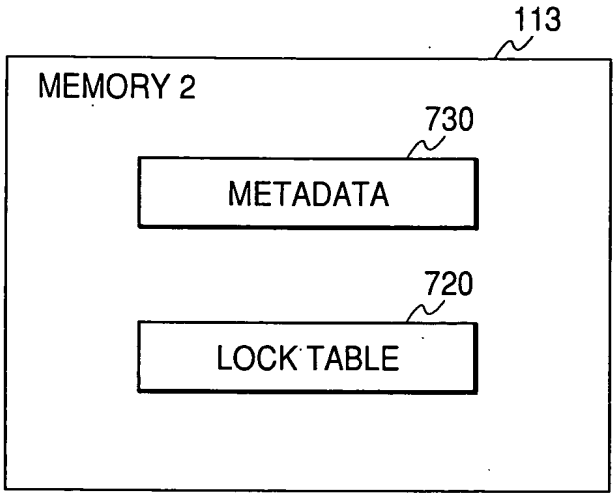

113
MEMORY 2
730
METADATA
720
LOCK TABLE

FIG. 10

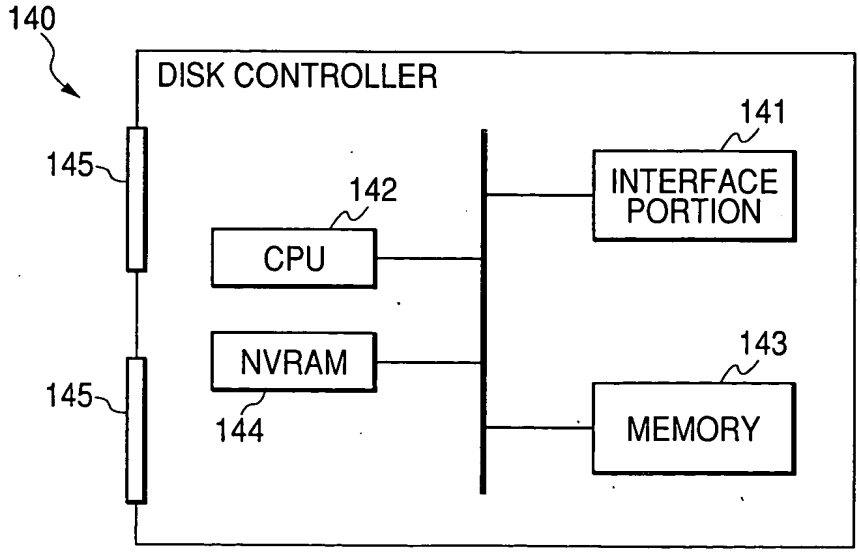

140
DISK CONTROLLER
141
145
142
INTERFACE PORTION
CPU
NVRAM
143
145
144
MEMORY

FIG. 11

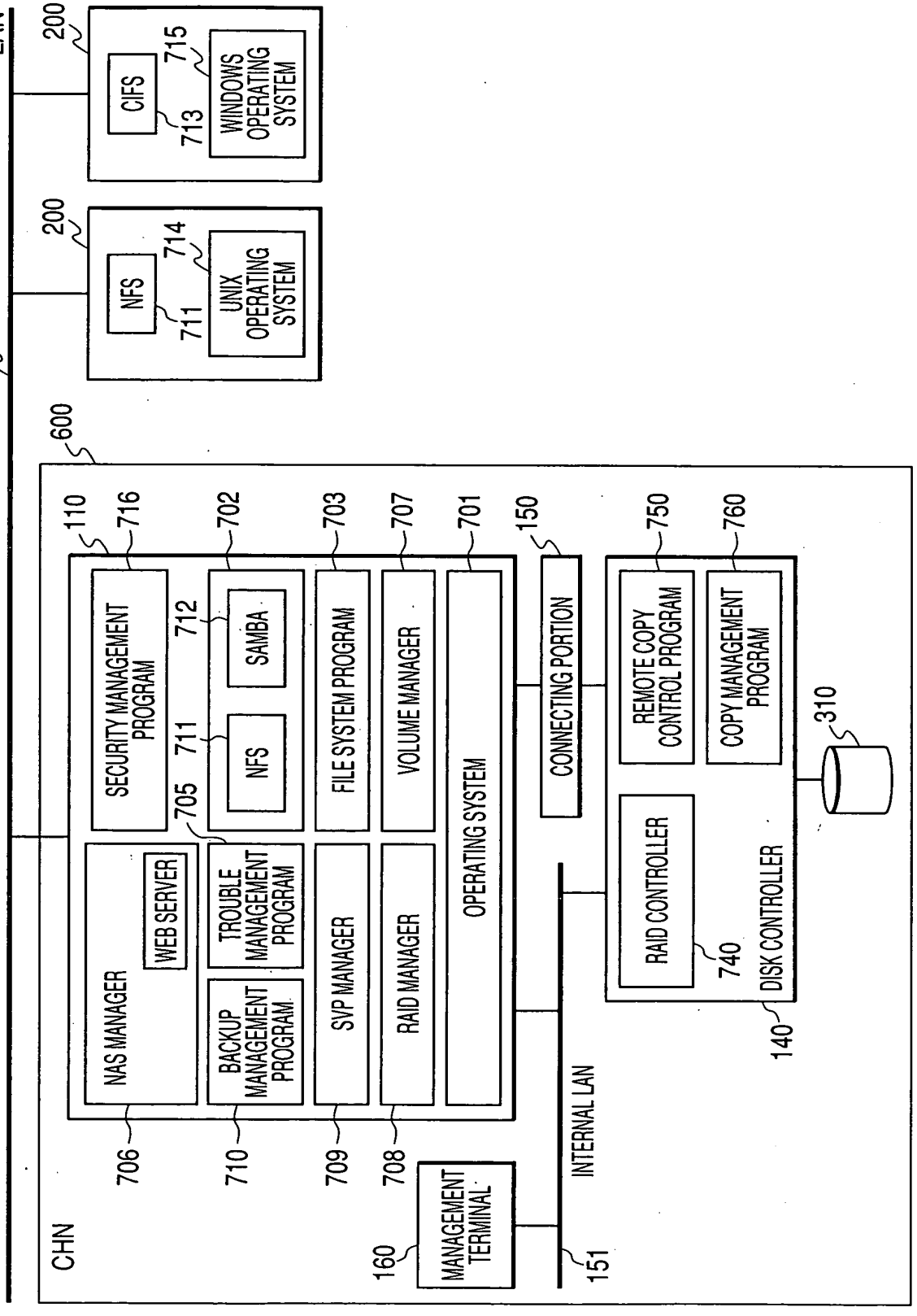

LAN
400
200
CIFS
713
715
WINDOWS OPERATING SYSTEM
200
NFS
711
714
UNIX OPERATING SYSTEM
600
CHN
110
716
SECURITY MANAGEMENT PROGRAM
NAS MANAGER
WEB SERVER
705
706
702
712
SAMBA
711
NFS
BACKUP MANAGEMENT PROGRAM
710
TROUBLE MANAGEMENT PROGRAM
703
FILE SYSTEM PROGRAM
709
SVP MANAGER
707
VOLUME MANAGER
708
RAID MANAGER
701
OPERATING SYSTEM
150
CONNECTING PORTION
750
REMOTE COPY CONTROL PROGRAM
760
COPY MANAGEMENT PROGRAM
310
RAID CONTROLLER
740
DISK CONTROLLER
140
160
MANAGEMENT TERMINAL
INTERNAL LAN
151

FIG. 12

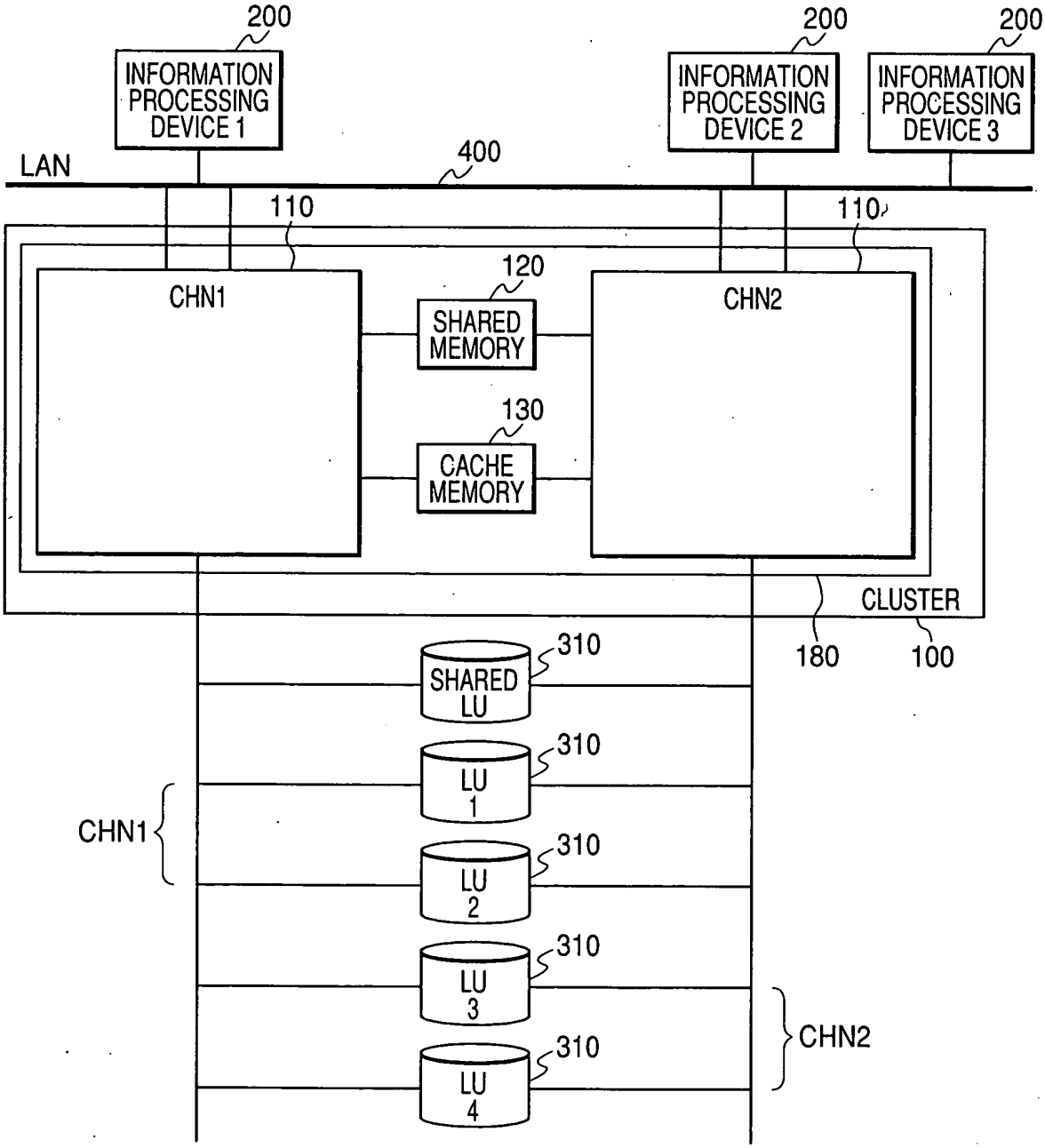

200
INFORMATION PROCESSING DEVICE 1
200
INFORMATION PROCESSING DEVICE 2
200
INFORMATION PROCESSING DEVICE 3
LAN
400
110
110
120
SHARED MEMORY
CHN1
CHN2
130
CACHE MEMORY
CLUSTER
180
100
310
SHARED LU
310
LU 1
CHN1
310
LU 2
310
LU 3
CHN2
310
LU 4

FIG. 13

730

METADATA

FILE NAME	HEAD ADDRESS	CAPACITY	OWNER	RENEWAL TIME
A	7BSA	200MB	X	0 : 00
B	05BF	50MB	X	7 : 57
C	1F30	100MB	Y	9 : 15
D	470B	100MB	Z	15 : 20
⋮	⋮	⋮	⋮	⋮

FIG. 14

721

FILE LOCK TABLE

FILE NAME	LOCK STATE
A	UNDER LOCK
B	—
C	—
D	UNDER LOCK
⋮	⋮

722

LU LOCK TABLE

LU	LOCK STATE
SHARING	—
1	UNDER LOCK
2	—
⋮	⋮

FIG. 15

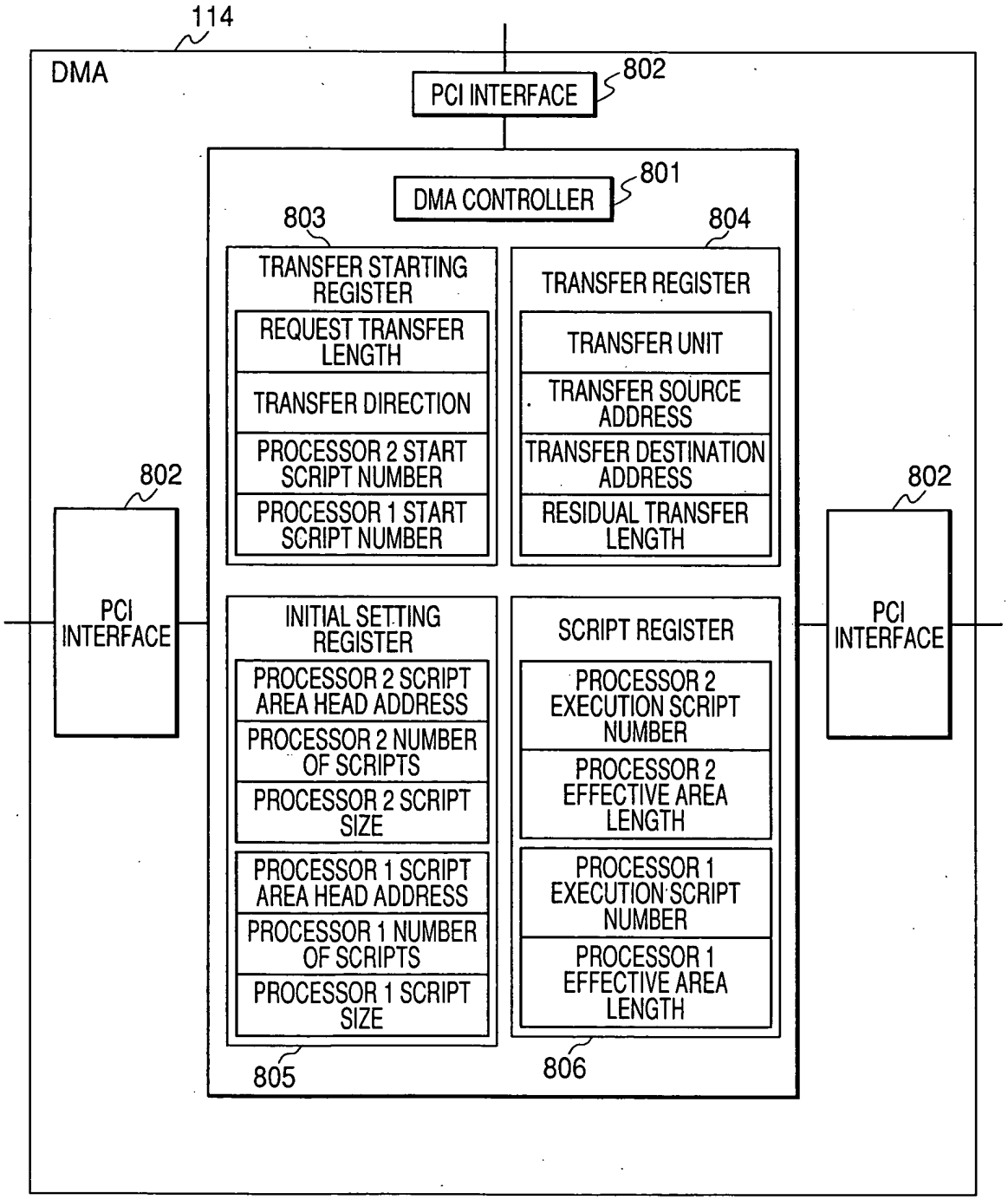

114
DMA
PCI INTERFACE
802
DMA CONTROLLER
801
803
TRANSFER STARTING REGISTER
REQUEST TRANSFER LENGTH
TRANSFER DIRECTION
PROCESSOR 2 START SCRIPT NUMBER
PROCESSOR 1 START SCRIPT NUMBER
804
TRANSFER REGISTER
TRANSFER UNIT
TRANSFER SOURCE ADDRESS
TRANSFER DESTINATION ADDRESS
RESIDUAL TRANSFER LENGTH
802
PCI INTERFACE
INITIAL SETTING REGISTER
PROCESSOR 2 SCRIPT AREA HEAD ADDRESS
PROCESSOR 2 NUMBER OF SCRIPTS
PROCESSOR 2 SCRIPT SIZE
PROCESSOR 1 SCRIPT AREA HEAD ADDRESS
PROCESSOR 1 NUMBER OF SCRIPTS
PROCESSOR 1 SCRIPT SIZE
805
SCRIPT REGISTER
PROCESSOR 2 EXECUTION SCRIPT NUMBER
PROCESSOR 2 EFFECTIVE AREA LENGTH
PROCESSOR 1 EXECUTION SCRIPT NUMBER
PROCESSOR 1 EFFECTIVE AREA LENGTH
806
802
PCI INTERFACE

FIG. 16

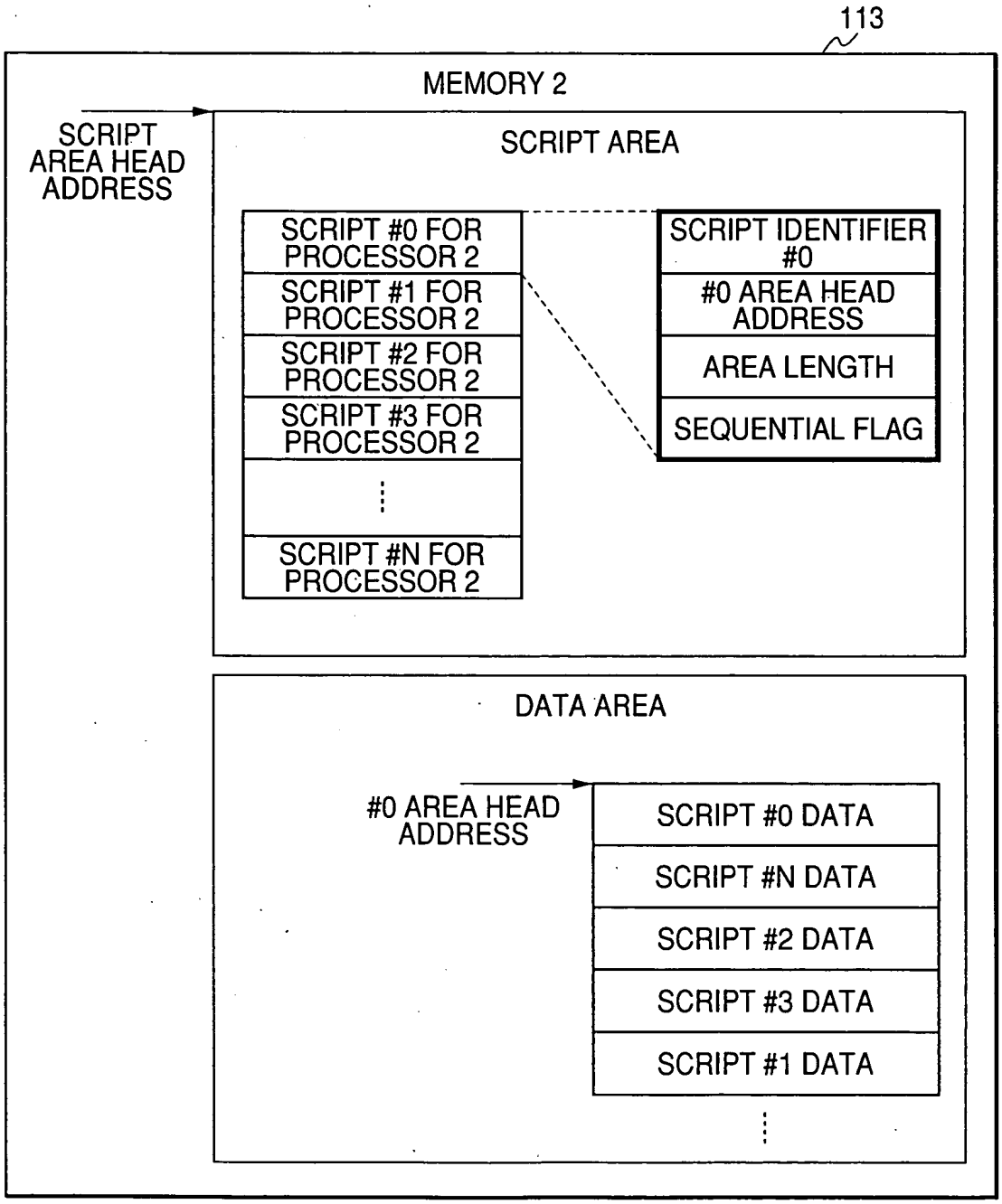

113
MEMORY 2
SCRIPT AREA HEAD ADDRESS
SCRIPT AREA
SCRIPT #0 FOR PROCESSOR 2
SCRIPT #1 FOR PROCESSOR 2
SCRIPT #2 FOR PROCESSOR 2
SCRIPT #3 FOR PROCESSOR 2
SCRIPT #N FOR PROCESSOR 2
SCRIPT IDENTIFIER #0
#0 AREA HEAD ADDRESS
AREA LENGTH
SEQUENTIAL FLAG
DATA AREA
#0 AREA HEAD ADDRESS
SCRIPT #0 DATA
SCRIPT #N DATA
SCRIPT #2 DATA
SCRIPT #3 DATA
SCRIPT #1 DATA

FIG. 17

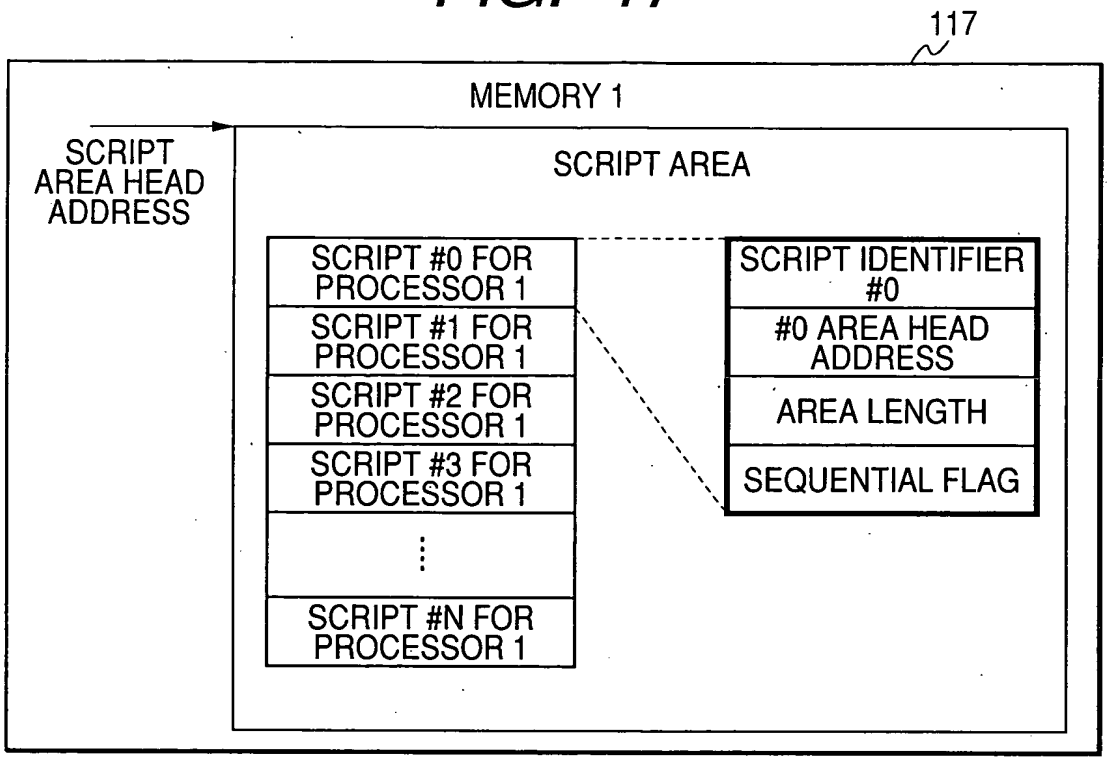

117
MEMORY 1
SCRIPT AREA HEAD ADDRESS
SCRIPT AREA
SCRIPT #0 FOR PROCESSOR 1
SCRIPT #1 FOR PROCESSOR 1
SCRIPT #2 FOR PROCESSOR 1
SCRIPT #3 FOR PROCESSOR 1
SCRIPT #N FOR PROCESSOR 1
SCRIPT IDENTIFIER #0
#0 AREA HEAD ADDRESS
AREA LENGTH
SEQUENTIAL FLAG

FIG. 18

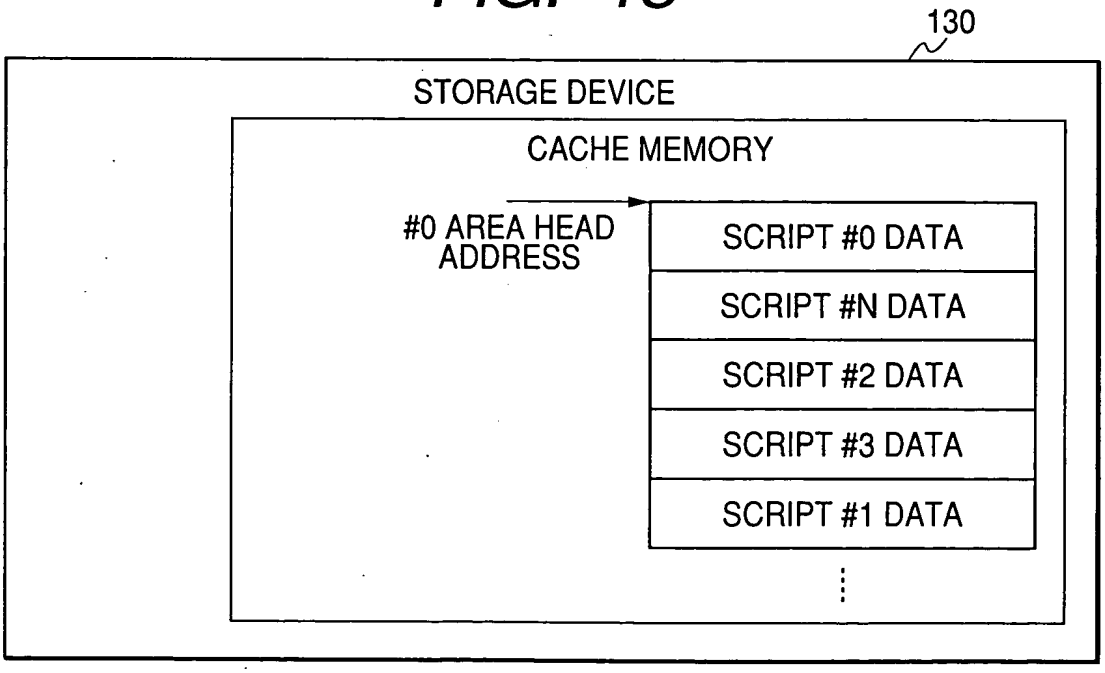

130
STORAGE DEVICE
CACHE MEMORY
#0 AREA HEAD ADDRESS
SCRIPT #0 DATA
SCRIPT #N DATA
SCRIPT #2 DATA
SCRIPT #3 DATA
SCRIPT #1 DATA

FIG. 19

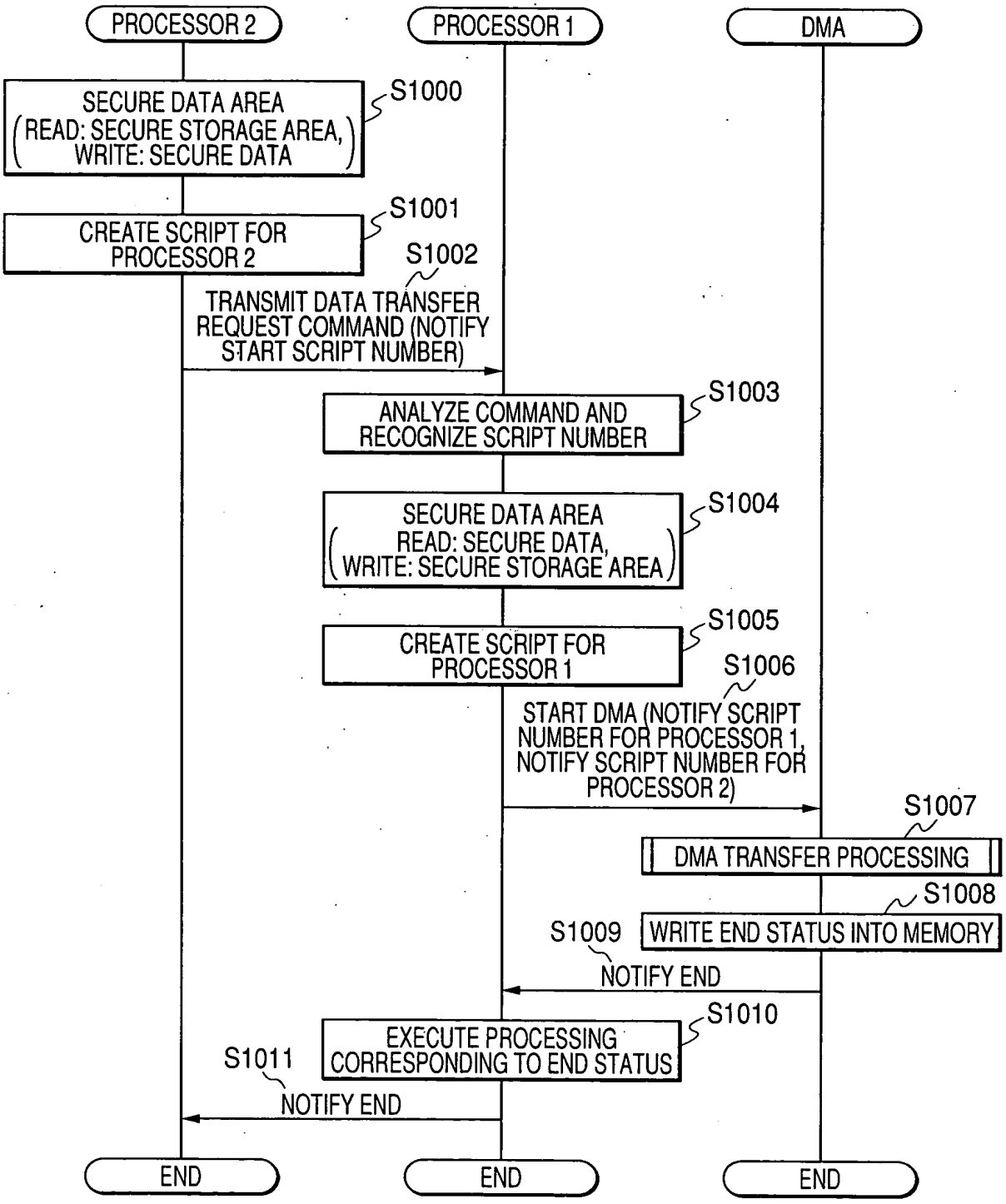

PROCESSOR 2
PROCESSOR 1
DMA
SECURE DATA AREA (READ: SECURE STORAGE AREA, WRITE: SECURE DATA
S1000
CREATE SCRIPT FOR PROCESSOR 2
S1001
S1002
TRANSMIT DATA TRANSFER REQUEST COMMAND (NOTIFY START SCRIPT NUMBER)
ANALYZE COMMAND AND RECOGNIZE SCRIPT NUMBER
S1003
SECURE DATA AREA (READ: SECURE DATA, WRITE: SECURE STORAGE AREA)
S1004
CREATE SCRIPT FOR PROCESSOR 1
S1005
S1006
START DMA (NOTIFY SCRIPT NUMBER FOR PROCESSOR 1, NOTIFY SCRIPT NUMBER FOR PROCESSOR 2)
S1007
DMA TRANSFER PROCESSING
S1008
WRITE END STATUS INTO MEMORY
S1009
NOTIFY END
EXECUTE PROCESSING CORRESPONDING TO END STATUS
S1010
S1011
NOTIFY END
END
END
END

FIG. 20

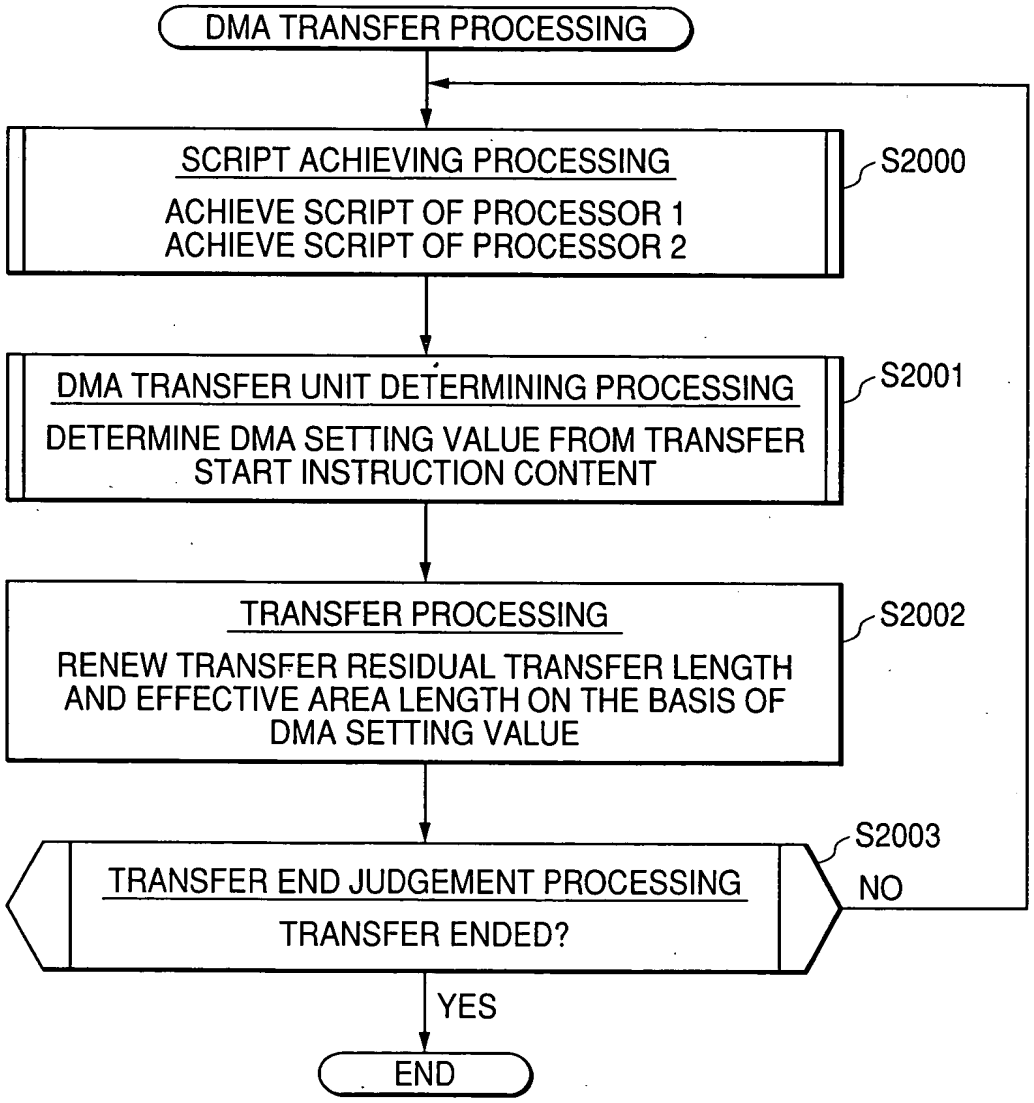

DMA TRANSFER PROCESSING
SCRIPT ACHIEVING PROCESSING
ACHIEVE SCRIPT OF PROCESSOR 1
ACHIEVE SCRIPT OF PROCESSOR 2
S2000
DMA TRANSFER UNIT DETERMINING PROCESSING
DETERMINE DMA SETTING VALUE FROM TRANSFER START INSTRUCTION CONTENT
S2001
TRANSFER PROCESSING
RENEW TRANSFER RESIDUAL TRANSFER LENGTH AND EFFECTIVE AREA LENGTH ON THE BASIS OF DMA SETTING VALUE
S2002
TRANSFER END JUDGEMENT PROCESSING
TRANSFER ENDED?
S2003
NO
YES
END

FIG. 21

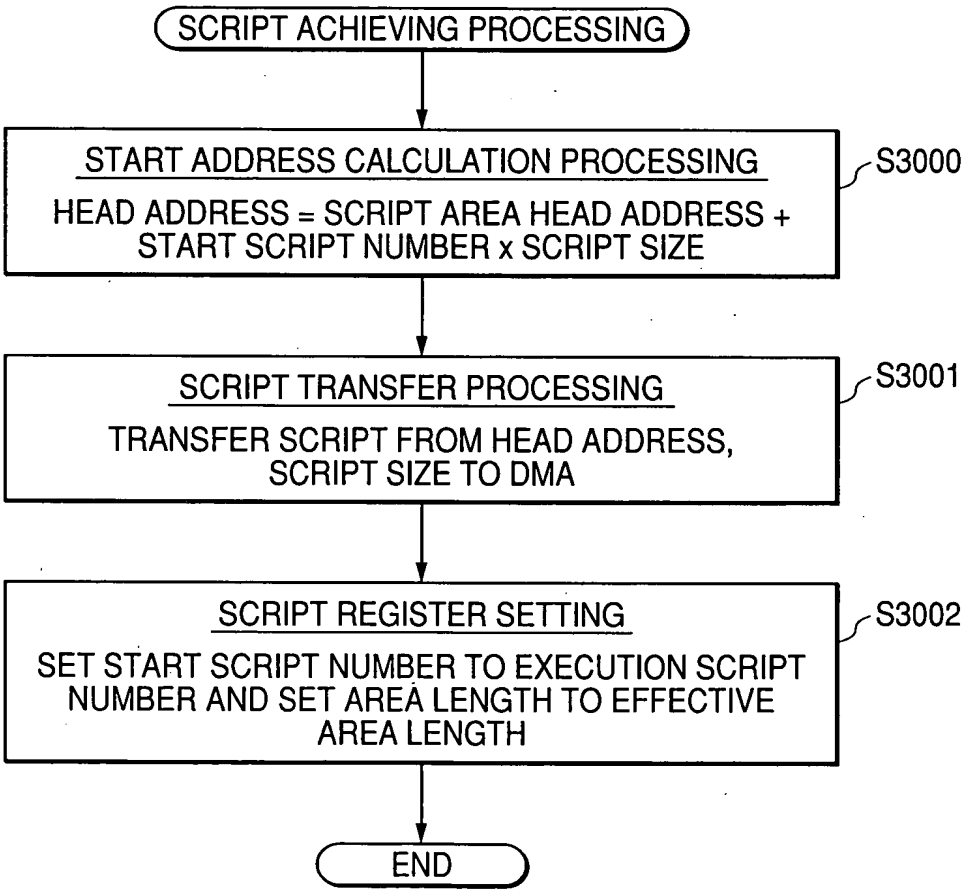

SCRIPT ACHIEVING PROCESSING
START ADDRESS CALCULATION PROCESSING
HEAD ADDRESS = SCRIPT AREA HEAD ADDRESS + START SCRIPT NUMBER x SCRIPT SIZE
S3000
SCRIPT TRANSFER PROCESSING
TRANSFER SCRIPT FROM HEAD ADDRESS, SCRIPT SIZE TO DMA
S3001
SCRIPT REGISTER SETTING
SET START SCRIPT NUMBER TO EXECUTION SCRIPT NUMBER AND SET AREA LENGTH TO EFFECTIVE AREA LENGTH
S3002
END

FIG. 22

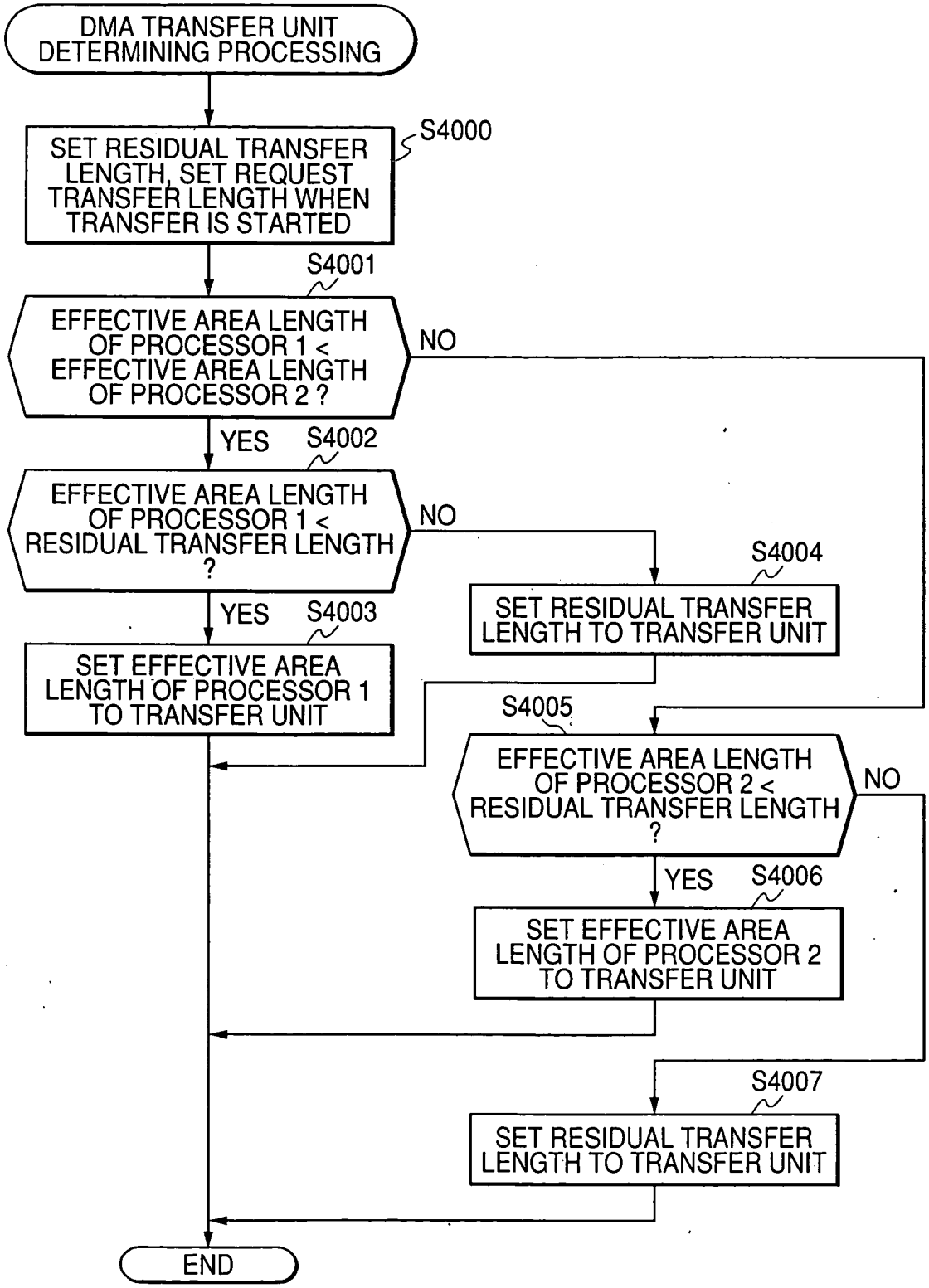

DMA TRANSFER UNIT DETERMINING PROCESSING
SET RESIDUAL TRANSFER LENGTH, SET REQUEST TRANSFER LENGTH WHEN TRANSFER IS STARTED
S4000
S4001
EFFECTIVE AREA LENGTH OF PROCESSOR 1 < EFFECTIVE AREA LENGTH OF PROCESSOR 2 ?
NO
YES
S4002
EFFECTIVE AREA LENGTH OF PROCESSOR 1 < RESIDUAL TRANSFER LENGTH ?
NO
YES
S4003
SET EFFECTIVE AREA LENGTH OF PROCESSOR 1 TO TRANSFER UNIT
S4004
SET RESIDUAL TRANSFER LENGTH TO TRANSFER UNIT
S4005
EFFECTIVE AREA LENGTH OF PROCESSOR 2 < RESIDUAL TRANSFER LENGTH ?
NO
YES
S4006
SET EFFECTIVE AREA LENGTH OF PROCESSOR 2 TO TRANSFER UNIT
S4007
SET RESIDUAL TRANSFER LENGTH TO TRANSFER UNIT
END

FIG. 23

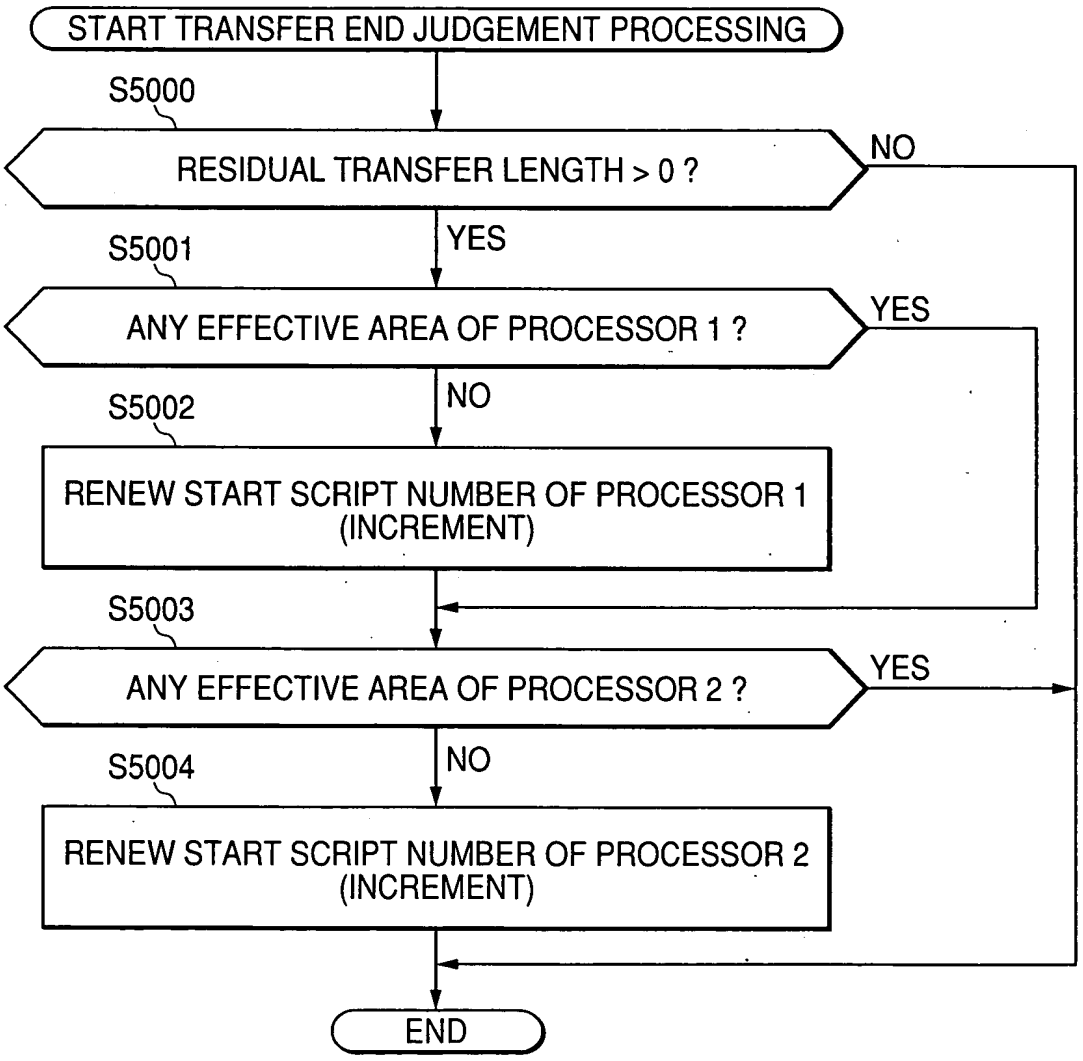

START TRANSFER END JUDGEMENT PROCESSING
S5000
RESIDUAL TRANSFER LENGTH > 0 ?
NO
YES
S5001
ANY EFFECTIVE AREA OF PROCESSOR 1 ?
YES
NO
S5002
RENEW START SCRIPT NUMBER OF PROCESSOR 1 (INCREMENT)
S5003
ANY EFFECTIVE AREA OF PROCESSOR 2 ?
YES
NO
S5004
RENEW START SCRIPT NUMBER OF PROCESSOR 2 (INCREMENT)
END

FIG. 24

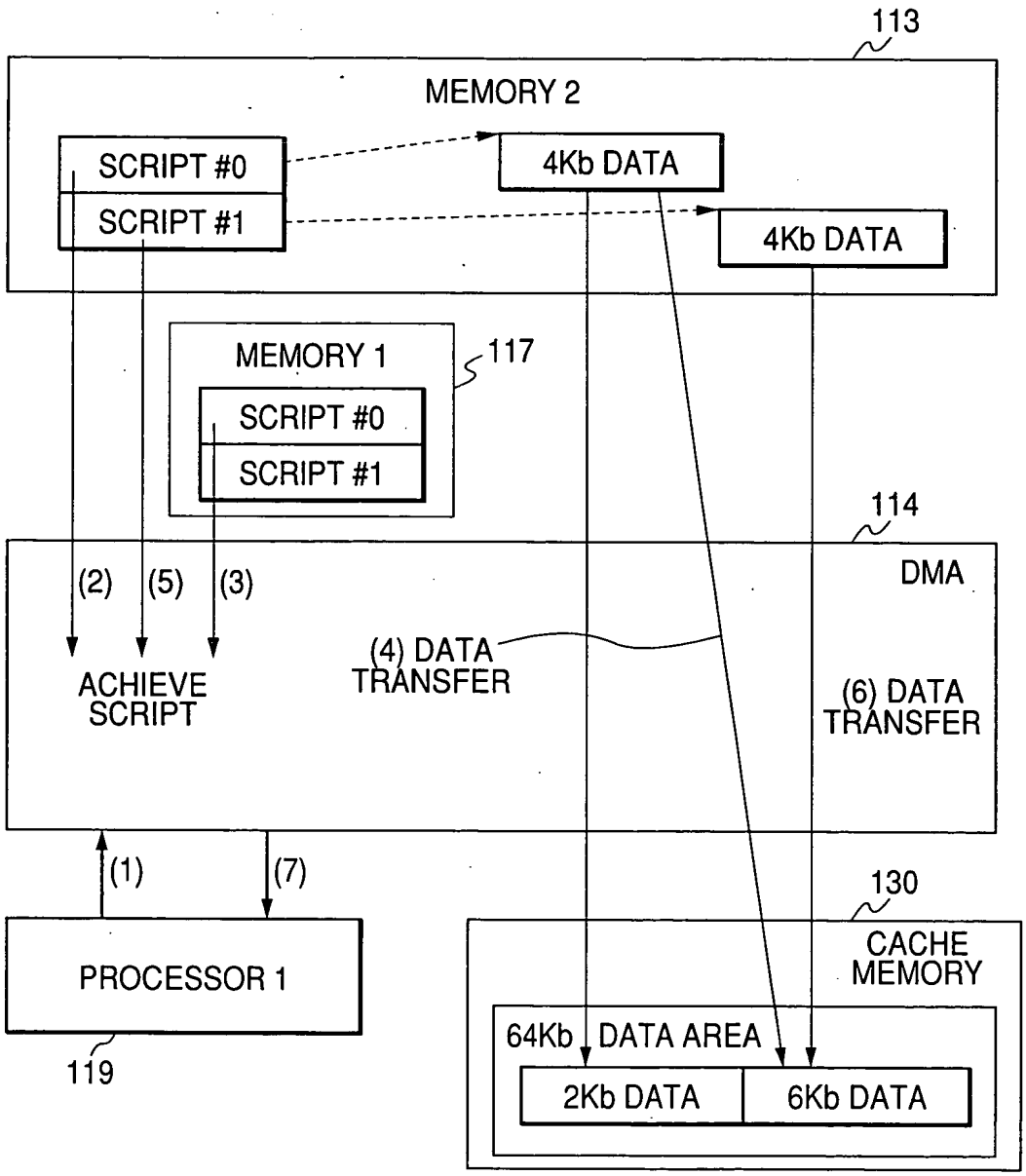

113
MEMORY 2
SCRIPT #0
SCRIPT #1
4Kb DATA
4Kb DATA
MEMORY 1
117
SCRIPT #0
SCRIPT #1
114
DMA
(2)
(5)
(3)
(4) DATA TRANSFER
ACHIEVE SCRIPT
(6) DATA TRANSFER
(1)
(7)
130
CACHE MEMORY
PROCESSOR 1
119
64Kb DATA AREA
2Kb DATA
6Kb DATA

FIG. 25

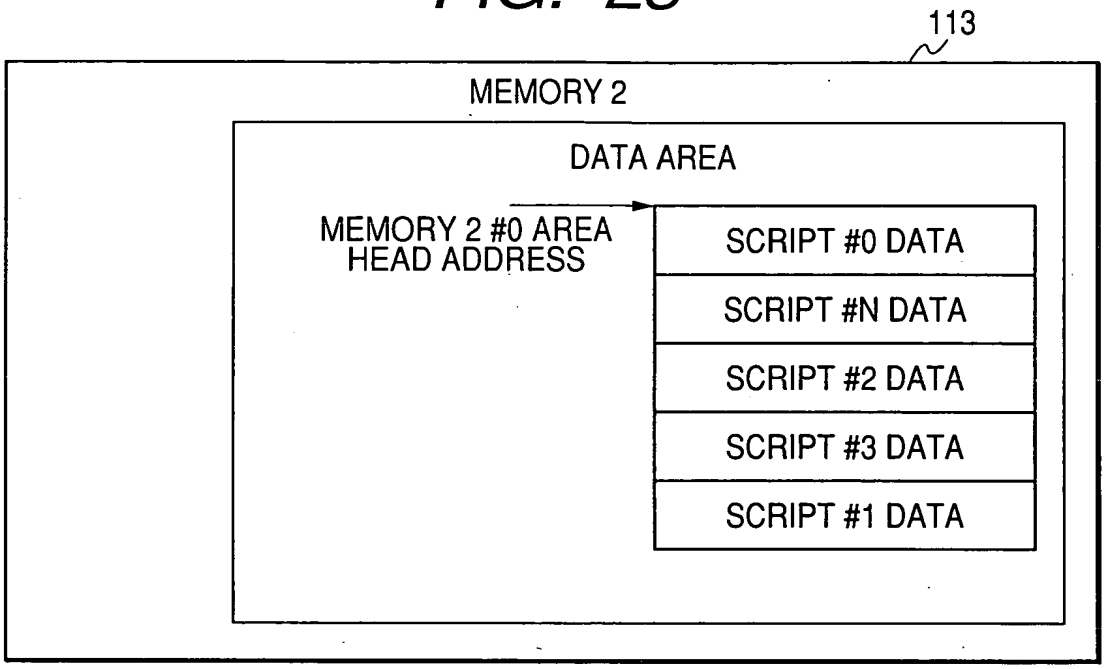

113
MEMORY 2
DATA AREA
MEMORY 2 #0 AREA HEAD ADDRESS
SCRIPT #0 DATA
SCRIPT #N DATA
SCRIPT #2 DATA
SCRIPT #3 DATA
SCRIPT #1 DATA

FIG. 26

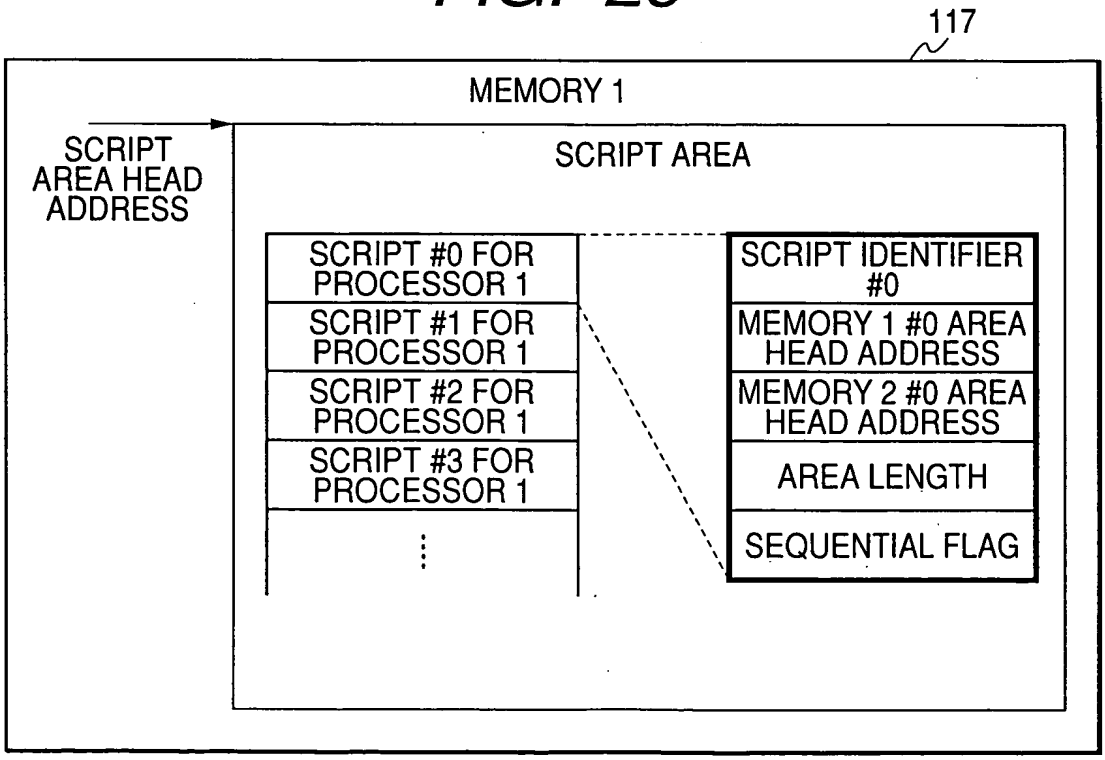

117
MEMORY 1
SCRIPT AREA HEAD ADDRESS
SCRIPT AREA
SCRIPT #0 FOR PROCESSOR 1
SCRIPT #1 FOR PROCESSOR 1
SCRIPT #2 FOR PROCESSOR 1
SCRIPT #3 FOR PROCESSOR 1
SCRIPT IDENTIFIER #0
MEMORY 1 #0 AREA HEAD ADDRESS
MEMORY 2 #0 AREA HEAD ADDRESS
AREA LENGTH
SEQUENTIAL FLAG

FIG. 27

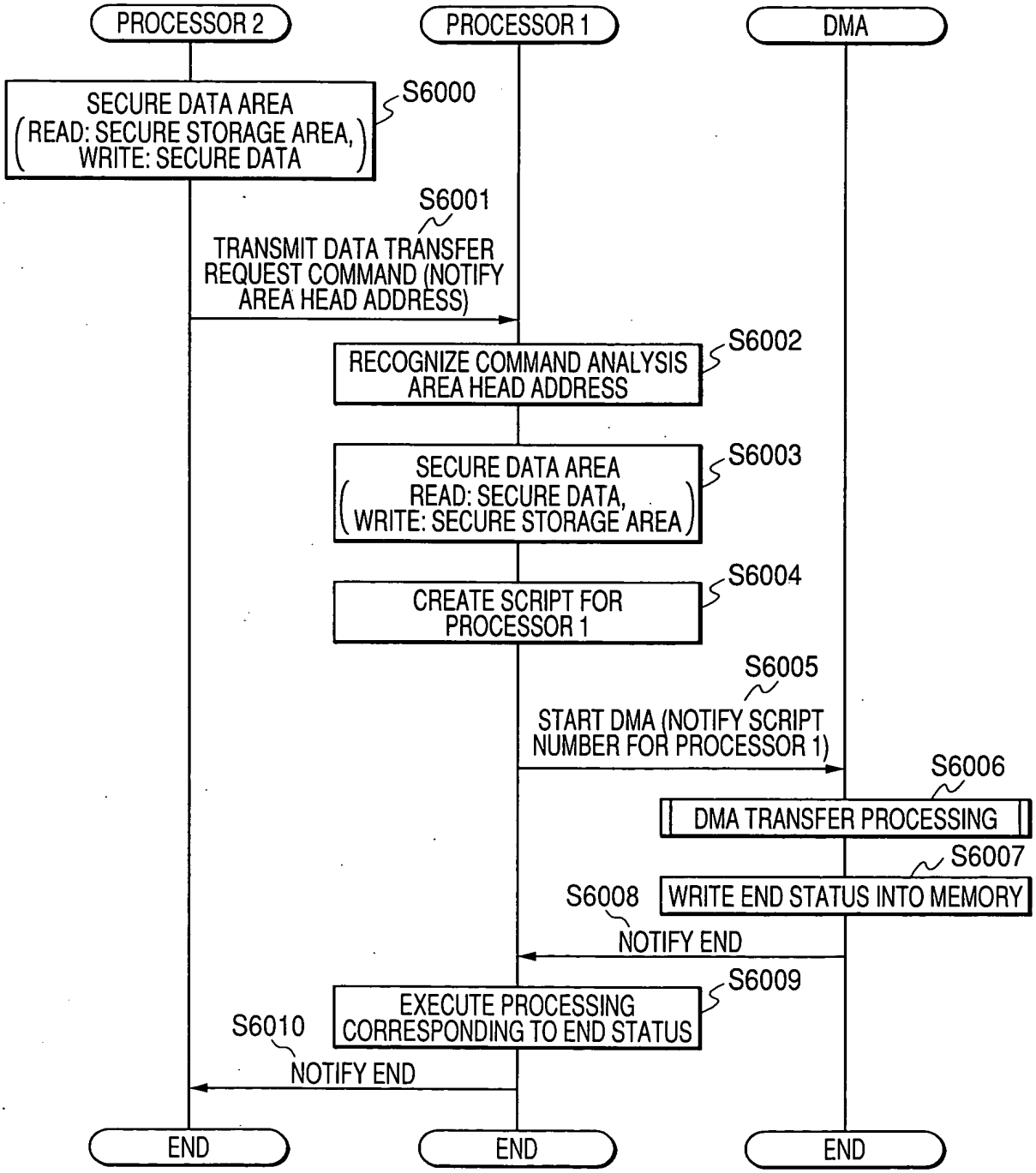
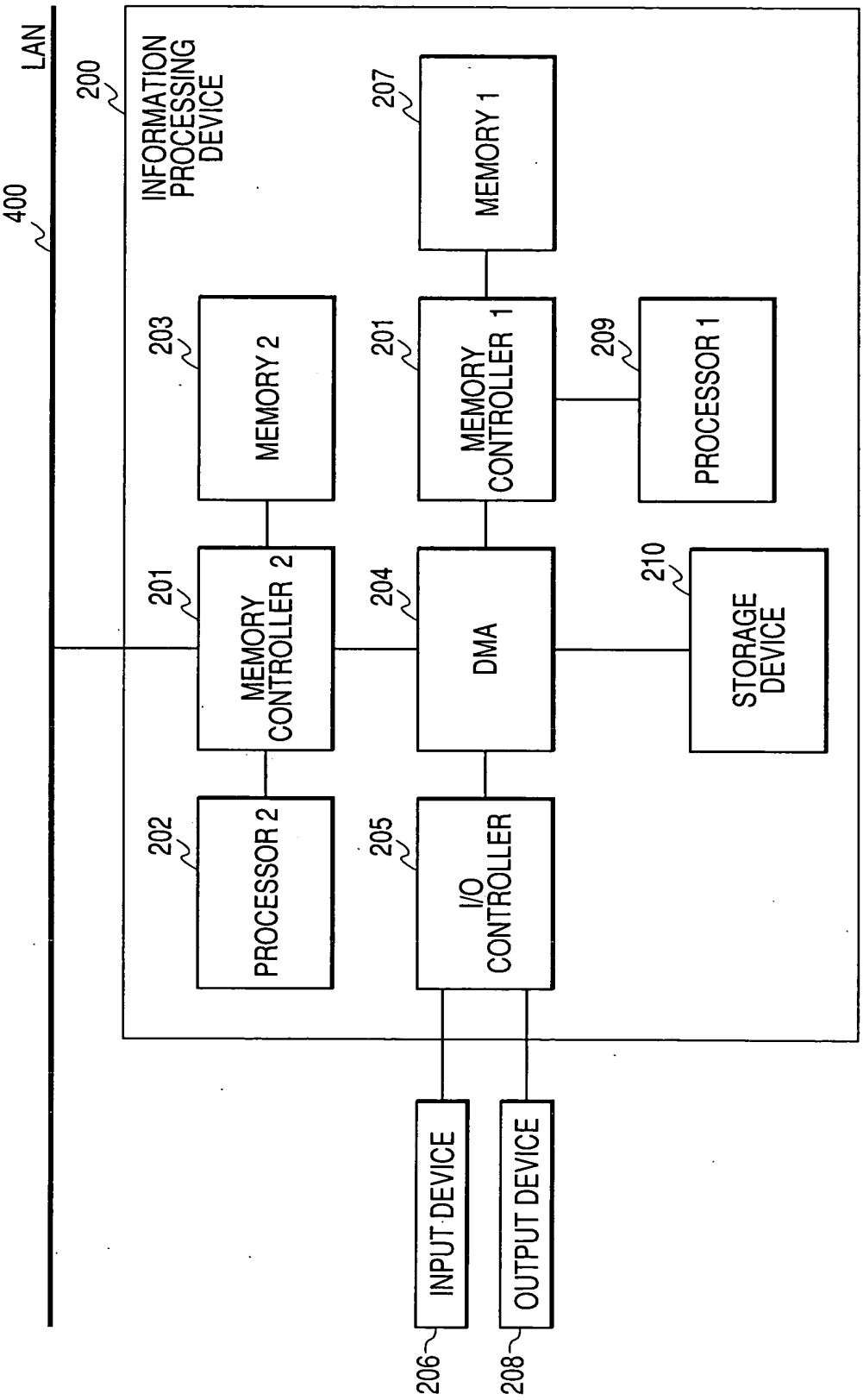

PROCESSOR 2
PROCESSOR 1
DMA
SECURE DATA AREA (READ: SECURE STORAGE AREA, WRITE: SECURE DATA
S6000
S6001
TRANSMIT DATA TRANSFER REQUEST COMMAND (NOTIFY AREA HEAD ADDRESS)
RECOGNIZE COMMAND ANALYSIS AREA HEAD ADDRESS
S6002
SECURE DATA AREA (READ: SECURE DATA, WRITE: SECURE STORAGE AREA
S6003
CREATE SCRIPT FOR PROCESSOR 1
S6004
S6005
START DMA (NOTIFY SCRIPT NUMBER FOR PROCESSOR 1)
S6006
DMA TRANSFER PROCESSING
S6007
WRITE END STATUS INTO MEMORY
S6008
NOTIFY END
EXECUTE PROCESSING CORRESPONDING TO END STATUS
S6009
S6010
NOTIFY END
END
END
END

FIG. 28


LAN
400
200
INFORMATION PROCESSING DEVICE
207
MEMORY 1
203
MEMORY 2
201
MEMORY CONTROLLER 1
209
PROCESSOR 1
201
MEMORY CONTROLLER 2
204
DMA
210
STORAGE DEVICE
202
PROCESSOR 2
205
I/O CONTROLLER
INPUT DEVICE
OUTPUT DEVICE
206
208